CLAIM AMENDMENTS

Claims 1-9 are currently pending in the application.

Please cancel claims 1-9 without prejudice or disclaimer as to the subject matter of claims 1-9.

Please add claims 10-29 as shown below.

The following listing of claims 10-29 will replace all prior versions, and listings, of claims in the application:

1.-9. (Cancelled)

10. (New) A processing system, comprising:

a device operable to decode a first program instruction into a first microcode instruction, said device further operable to decode a second program instruction into a second microcode instruction;

a circuit in electrical communication with said device, said circuit operable to process the first microcode instruction subsequent to a first decoding of the first program instruction by said device, said circuit further operable to process the second microcode instruction subsequent to a second decoding of the second program instruction by said device and a first processing of the first microcode instruction by said circuit;

wherein the first program instruction includes a first field defining a first jump type to be decoded by said device;

wherein the first program instruction further includes a second field defining a first destination address to be decoded by said device;

wherein the second program instruction includes a third field defining a second jump type to be decoded by said device; and

wherein the second program instruction excludes a fourth field defining a second destination address to be decoded by said device.

11. (New) The processing system of claim 10,

wherein said device is further operable to store the first destination address as a default-destination-address as a result of the first decoding of the first program instruction by said device; and

wherein said device is further operable to include the first destination address in the second microcode instruction as a result of the second decoding of the second program instruction by said device.

12. (New) The processing system of claim 10,

wherein the first program instruction includes a fifth field defining a first jump condition to be decoded by said device;

wherein the second program instruction excludes a sixth field defining a second jump condition to be decoded by said device.

13. (New) The processing system of claim 12,

wherein said device is further operable to store the first jump condition as a default-condition as a result of the first decoding of the first program instruction by said device; and

wherein said device is further operable to include the first jump condition in the second microcode instruction as a result of the second decoding of the second program instruction by said device.

14. (New) The processing system of claim 10,

wherein said device is further operable to decode a third program instruction into a third microcode instruction;

wherein said circuit is further operable to process the third microcode instruction subsequent to the first processing of the first microcode instruction by said circuit, prior to the second decoding of the second program instruction by said device and subsequent to a third decoding of the third program instruction by said device;

wherein the third program instruction includes a fifth field defining a first jump condition to be decoded by said device;

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wherein the second program instruction excludes a sixth field defining a second jump condition to be decoded by said device.

15. (New) The processing system of claim 14,

wherein said device is further operable to store the first jump condition as a default-condition as a result of the third decoding of the third program instruction by said device; and

wherein said device is further operable to include the first jump condition in the second microcode instruction as a result of the second decoding of the second program instruction by said device.

16. (New) The processing system of claim 10,

wherein the first jump type is one of a branch instruction or a call instruction.

17. (New) The processing system of claim 10,

wherein the second jump type is one of a branch instruction or a call instruction.

18. (New) A processing system, comprising:

a device operable to decode a first program instruction into a first microcode instruction, said device further operable to decode a second program instruction into a second microcode instruction;

a circuit in electrical communication with said device, said circuit operable to process the first microcode instruction subsequent to a first decoding of the first program instruction by said device, said circuit further operable to process the second microcode instruction subsequent to a second decoding of the second program instruction by said device and a first processing of the first microcode instruction by said circuit;

wherein the first program instruction includes a first field defining a first jump type to be decoded by said device;

wherein the first program instruction further includes a second field defining a first jump condition to be decoded by said device;

wherein the second program instruction includes a third field defining a second jump type to be decoded by said device; and

wherein the second program instruction excludes a fourth field defining a second jump condition to be decoded by said device.

19. (New) The processing system of claim 18,

wherein said device is further operable to store the first jump condition as a default-condition as a result of the first decoding of the first program instruction by said device; and

wherein said device is further operable to include the first jump condition in the second microcode instruction as a result of the second decoding of the second program instruction by said device.

20. (New) The processing system of claim 18,

wherein the first jump type is one of a branch instruction or a call instruction.

21. (New) The processing system of claim 18,

wherein the second jump type is one of a branch instruction or a call instruction.

22. (New) A processing system, comprising:

a device operable to decode a first program instruction into a first microcode instruction, said device further operable to decode a second program instruction into a second microcode instruction;

a circuit in electrical communication with said device, said circuit operable to process the first microcode instruction subsequent to a first decoding of the first program instruction by said device, said circuit further operable to process the second microcode instruction subsequent to a second decoding of the second program

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instruction by said device and a first processing of the first microcode instruction by said circuit;

wherein the first program instruction further includes a first field defining a first destination address to be decoded by said device;

wherein the second program instruction includes a second field defining a jump type to be decoded by said device; and

wherein the second program instruction excludes a third field defining a second destination address to be decoded by said device.

23. (New) The processing system of claim 22,

wherein said device is further operable to store the first destination address as a default-destination-address as a result of the first decoding of the first program instruction by said device; and

wherein said device is further operable to include the first destination address in the second microcode instruction as a result of the second decoding of the second program instruction by said device.

24. (New) The processing system of claim 23,

wherein the second program instruction excludes a fourth field defining a jump condition to be decoded by said device; and

wherein said device is further operable to include the jump condition in the second microcode instruction as a result of the second decoding of the second program instruction by said device

25. (New) The processing system of claim 22,

wherein the jump type is one of a branch instruction or a call instruction.

26. (New) A processing system, comprising:

a device operable to decode a first program instruction into a first microcode instruction, said device further operable to decode a second program instruction into a second microcode instruction;

a circuit in electrical communication with said device, said circuit operable to process the first microcode instruction subsequent to a first decoding of the first program instruction by said device, said circuit further operable to process the second microcode instruction subsequent to a second decoding of the second program instruction by said device and a first processing of the first microcode instruction by said circuit;

wherein the first program instruction further includes a first field defining a first jump condition to be decoded by said device;

wherein the second program instruction includes a second field defining a jump type to be decoded by said device; and

wherein the second program instruction excludes a third field defining a second jump condition to be decoded by said device.

27. (New) The processing system of claim 26,

wherein said device is further operable to store the first jump condition as a default-condition as a result of the first decoding of the first program instruction by said device; and

wherein said device is further operable to include the first jump condition in the second microcode instruction as a result of the second decoding of the second program instruction by said device.

28. (New) The processing system of claim 27,

wherein the second program instruction excludes a fourth field defining a destination address to be decoded by said device; and

wherein said device is further operable to include the destination address in the second microcode instruction as a result of the second decoding of the second program instruction by said device.

29. (New) The processing system of claim 26,

wherein the jump type is one of a branch instruction or a call instruction.